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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/516,004
Filing Date: February 29, 2000
Appellant(s): KIZILYALLI ET AL.

Mark J. Marcelli
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/16/2004.

(1) ***Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

(2) ***Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) ***Status of Claims***

The statement of the status of the claims contained in the brief is correct.

(4) ***Status of Amendments After Final***

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) ***Summary of Invention***

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 6-11 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

6,194,748	Yu	2-2001
5,292,673	Shinriki et al.	3-1994
5,596,214	Endo	1-1997

Applicant Admitted Prior Art (AAPA), page 7, lines 3-9.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 6-8 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification recites forming self-aligned source and drain regions. The drawings illustrate that subsequent processing

steps diffuse the source and drain regions under the gate, such that the source and drain regions in the final structure are not self-aligned with the gate electrode. Claim 6 recites "source region and the drain region directly self-aligned with the gate structure" forming "an operable self-aligned field effect transistor". There is no support for operable self-aligned transistor, wherein the source region and the drain region are directly self-aligned with the gate structure, as recited in claim 6.

2. Claims 6-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu.
Yu teaches in figure 1 an integrated circuit comprising a semiconductor material 14 of the first conductivity type, a FET gate structure on the semiconductor material comprising a conductive layer 36 and an amorphous tantalum pentoxide 34 (column 5, lines 50-55) formed between the conductive layer and the semiconductor material and having a dielectric constant greater than 5, self-aligned source and drain regions 17, 19 of the second conductivity type along the surface region of the semiconductor material configured to form an operable FET, and being directly self aligned with the gate structure.
Although Yu does not state that self-aligned source and drain regions are formed self-aligned with the gate structure, this feature is inherent in Yu's structure, for the following reasons. Appellant provides a text book definition of self-aligned structure (Wolf, "Silicon Processing for the VLSI Era"). A self-aligned structure is defined as a structure wherein the gate serves as a mask during the formation of source and drain regions. "These are self-aligned source and drain regions" (appellant's brief, page 11). Yu's device is formed in an identical process. Yu forms gate electrode 18, and then forms source and drain regions 22, 24 (column 6, lines 3-10). Clearly, gate electrode 18 acts as a mask while implanting or diffusing source and drain regions 22, 24, as the ions of the

source and drain regions are not present under a portion of the gate (see figure 3). Therefore, Yu's structure is a self-aligned structure, wherein self-aligned source and drain regions are formed self-aligned with the gate structure.
In the alternative, forming source and drain regions self-aligned with the gate structure (i.e. using the gate as a mask while implanting or diffusing the source and drain regions) are processing limitations which do not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced, since the source and drain regions do not stay self-aligned with the sidewalls of the gate. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

3. Claims 6-7 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Applicant Admitted Prior Art (AAPA) or Shinriki et al.
Yu teaches in figure 1 an integrated circuit comprising a semiconductor material 14 of the first conductivity type, a FET gate structure on the semiconductor material comprising a conductive layer 36 and an amorphous tantalum pentoxide 34 (column 5, lines 50-55) formed between the conductive layer and the semiconductor material and having a

dielectric constant greater than 5, self-aligned source and drain regions 17, 19 of the second conductivity type along the surface region of the semiconductor material configured to form a self-aligned operable FET, and being directly self-aligned with the gate structure.

Yu does not explicitly state that the source and drain regions are self-aligned source and drain regions.

Yu teaches source and drain regions can be formed self-aligned with the gate structure (column 1, lines 6-27).

Yu further teaches forming gate electrode 18, and then forming source and drain region 22, 24 (column 6, lines 3-10). Clearly, gate electrode 18 acts as a mask while implanting or diffusing source and drain region 22, 24, as the ions of the source and drain regions are not present under a portion of the gate (see figure 3).

AAPA teaches that it is conventional to form self-aligned source and drain regions (page 7, lines 3-9). Shinriki et al. teach in figure 6a self-aligned source and drain regions 11 (column 5, lines 30-31).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain regions of Yu's device by using the gate as a mask such that the source and drain regions are self-aligned with the gate structure, because it is conventional in the art to form self-aligned source and drain regions in order to simplify the processing steps of making the device by using the gate as a mask. Note that the processing step of forming self-aligned source and drain regions by using the gate as a mask is conventional in the art, of which judicial notice is taken.

Regarding claims 9-11, the claimed limitations of a gate leakage current being less than one milliamp per cm(-2) during operation are inherent in Yu's device, because it is known that a structure having a gate dielectric of an amorphous tantalum pentoxide which has a dielectric constant greater than 5, would produce a gate leakage current being less than one milliamp per cm(-2) (see specification, page 8, lines 8-10).

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, AAPA and Shinriki et al., as applied to claim 6 above, and further in view of Endo (5,596,214). Yu, AAPA and Shinriki et al. teach substantially the entire claimed structure, as applied to claim 6 above, except a layer of silicon oxide disposed between the insulative layer and the surface region.

Endo teaches in figure 3a layer of silicon oxide disposed between the insulative layer and the surface region (column 14, lines 57-58). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a layer of silicon oxide disposed between the insulative layer and the surface region in prior art's device in order to reduce the gate leakage current of the device by providing an additional insulation layer.

(11) Response to Argument

1. Appellant argues on pages 6-9 that although "the self-aligned source and drain regions may include a slight overlap region with the gate as illustrated in figures 1-3" (page 7, fourth paragraph of the appeal brief), there is support for operable self-aligned transistor, wherein the source region and the drain region are directly self-aligned with the gate structure, as recited in claim 6. Appellant further argues that "the source and drain

regions remain self-aligned as shown in figures 2 and 3" (page 7, fourth paragraph of the appeal brief).

Although figure 2 depict the source and drain regions being formed self-aligned with the gate structure, the device of figure 2 is not operable, since no reflective/protective layer is present over the gate structure and further processing steps are required to render the device operable. The further processing steps required to render the device operable diffuse the source and drain regions under the gate, and thus obtaining a device wherein the source and drain regions are not self-aligned with the gate. The device of figures 1 and 3 clearly does not comprise self-aligned source and drain regions as the subsequent processing steps diffuse the source and drain regions under the gate.

2. Appellant argues on page 8 that the embodiment of figure 5 is a different embodiment from that illustrated in figures 1-3, and "Figure 5 does not suggest that the embodiment shown in Figures 1, 2 or 3, has been further processed such that initially self-aligned source and drain regions have become transformed to being non-self-aligned".

The specification recites on page 5, lines 19-20: "Figure 5 illustrates the wafer of figure 1 during a subsequent phase of manufacture;". Therefore, the embodiment shown in figures 1, 2 or 3, has been further processed such that the initially self-aligned source and drain regions (as depicted in figure 2) have become transformed to being even further non-self-aligned with the introduction of the LDD region.

3. Appellant argues on pages 9-13 that Yu does not teach source and drain regions being formed directly self-aligned with the gate structure, because forming self-aligned source and drain regions is a structural limitation and not a process limitation.

Appellant provides a text book definition of self-aligned structure (Wolf, "Silicon Processing for the VLSI Era"). A self-aligned structure is defined as a structure wherein the gate serves as a mask during the formation of source and drain regions. "These are self-aligned source and drain regions .... The only overlap of the source and drain regions being that due to lateral diffusion of the dopant atoms" (appellant's brief, page 11). That is, in a self-aligned structure the source and drain regions are formed by using the gate as a mask, wherein during subsequent processing steps the source and drain regions overlap with the gate structure (i.e. the source and drain regions are not aligned with the sidewalls of the gate electrode). Appellant did not explicitly disclose why a self-aligned structure is not a processing limitation, and what is the difference between a device having source and drain regions which are formed by using the gate as a mask and between a device having source and drain regions which are formed by not using the gate as a mask. In fact, there is no structural difference between a device having source and drain regions which are formed by using the gate as a mask and between a device having source and drain regions which are formed by not using the gate as a mask. Even appellant does not disclose any structural distinction between the two scenarios. Appellant merely recites that it is common in current semiconductor processing to form the source/drain regions 21, 22 self-aligned with respect to the gate structure, whereas other techniques may also be used to provide dopant to the source/drain regions 21, 22 (specification, page 7, lines 3-9). There is no teaching that one structure is structurally different or superior to the other.

Furthermore, Yu's structure is formed in a process identical to that used by appellant. Yu forms gate electrode 18, and then forms source and drain region 22, 24 (column 6, lines 3-10). Clearly, gate electrode 18 acts as a mask while implanting or diffusing source and drain region 22, 24, as the ions of the source and drain regions are

not present under a portion of the gate (see figure 3). Therefore, Yu's structure is a self-aligned structure, wherein self-aligned source and drain regions are formed self-aligned with the gate structure.

4. Appellant provides "evidence" on pages 11-12 that forming self-aligned source and drain regions is a structural limitation and not a process limitation by reciting numerous passages and U.S. patents wherein devices are formed and claimed as having self-aligned source and drain regions.

Of course, claiming a final structure wherein the source and drain regions are self-aligned with the gate structure is structurally different from a device whose final structure does not include source and drain regions self-aligned with the gate structure. However, claiming a device formed by using the gate as a mask to obtain self-aligned source and drain regions and then diffusing the source and drain regions under the gate such that the source and drain regions are not self-aligned with the gate, is not structurally different from a device wherein the source and drain regions are formed without using the gate as a mask.

5. Appellant argues on page 14 that "Yu does not and can not produce self-aligned source and drain regions because Yu's gates must be formed after source/drain regions have been formed and annealed".

Yu clearly states that the source/drain regions are formed after forming the gate electrode (column 6, lines 3-10). Therefore, Yu must teach self-aligned source and drain regions.

6. Appellant argues on page 15 that although prior art teaches that self-aligned source and drain regions are desirable, this feature is not achievable with an amorphous insulative layer in an operable transistor in Yu's device.

Yu teaches an operable transistor comprising an amorphous insulative layer. Yu further teaches forming gate electrode 18, and then forming source and drain region 22, 24 (column 6, lines 3-10). The advantages of forming self-aligned source and drain regions are known and acknowledged by appellant. Forming self-aligned source and drain regions means the gate electrode is used as a mask while implanting or diffusing the source and drain region. Since Yu forms the gate electrode before forming the source and drain regions, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the gate as a mask while implanting or diffusing the source and drain regions, and thus obtaining a self-aligned structure.

Furthermore, the examiner took the official notice that it is conventional to use the gate as a mask to form a self-aligned source and drain regions in Yu's device. Appellant did not seasonably traverse the well known statement during examination. If appellant does not seasonably traverse the well known statement during examination, then the object of the well known statement is taken to be admitted prior art. In re Chevenard , 139 F.2d 71, 60 USPQ 239 (CCPA 1943)

Moreover, even appellant states that forming the source/drain regions self-aligned with respect to the gate structure is common to current semiconductor processing (specification, page 7, lines 3-9). Therefore, it would have been obvious to an artisan to form a self-aligned structure, as claimed.

7. Appellant argues on page 15 that there is no motivation to combine Shinriki et al. and AAPA with Yu.

AAPA teaches that it is conventional to form self-aligned source and drain regions (page 7, lines 3-9). Shinriki et al. teach in figure 6a self-aligned source and drain regions 11 (column 5, lines 30-31). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the gate as a mask to form the source and drain regions of Yu's device such that the source and drain regions are self-aligned with the gate structure, in order to simplify the processing steps of making the device. Using the gate as a mask eliminates the need for additional masking steps to form the source and drain regions.

8. Appellant argues on pages 15-16 that Yu does not teach the claimed limitation of a gate leakage current being less than one milliamp per cm(-2) during operation, as recited in claim 9, because the examiner stated that Yu's structure is different from the claimed structure and none of the cited references disclose a gate leakage current being less than one milliamp per cm(-2) during operation.

The issue is whether the device of Yu, AAPA and Shinriki et al. includes the limitations of a gate leakage current being less than one milliamp per cm(-2) during operation. It is known that a structure having a gate dielectric of an amorphous tantalum pentoxide which has a dielectric constant greater than 5, would produce a gate leakage current being less than one milliamp per cm(-2). Appellant teaches that leakage currents at or below one milliamp per cm are achievable when the temperature of the Ta2O5 is kept below the threshold at which it would transition out of the amorphous state (specification, page 8, lines 8-10). Since the device of Yu, AAPA and Shinriki et al. comprises a gate dielectric of an amorphous tantalum pentoxide which has a dielectric constant greater than 5, then the device of Yu, AAPA and Shinriki et al. includes a gate leakage current being less than one milliamp per cm(-2) during operation, as claimed.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted

Ori Nadav

October 16, 2004

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